



LEO SPACE PHOTONICS

Development of VCSEL transceiver chipset and module for intra-satellite optical interconnects in the framework of H2020-SPACE-SIPHODIAS

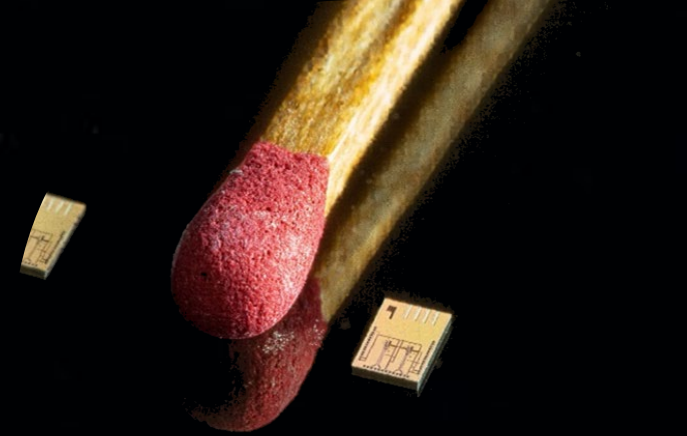
Workshop on optical interconnects for space and aeronautic applications
Toulouse
15/11/22

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About LEO Space Photonics

- Start-up founded in Feb. 2018 based in Attica Technology Park, Athens, Greece



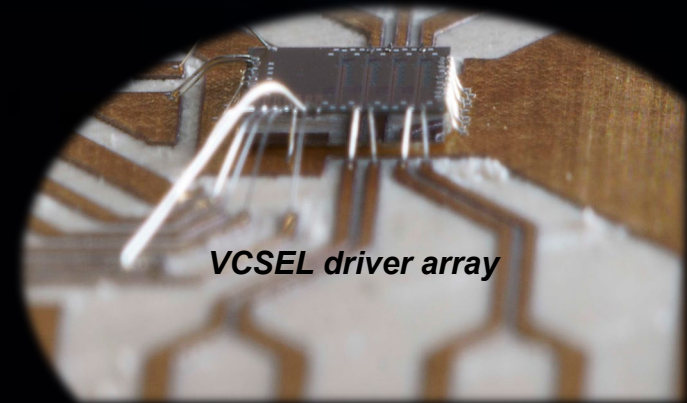
SiPh Coherent Receiver

- Developer of Electronic & Photonic TRx solutions for SatCom:

- Intra-satellite fiber optic links
- Free-space optical inter-satellite links

- Leading EC funded R&D programmes on:

- VCSEL TRx for on-board optical interconnects (H2020-SPACE-SIPHODIAS)
- PIC TRx for satellite constellations (H2020-SPACE-ORIONAS)



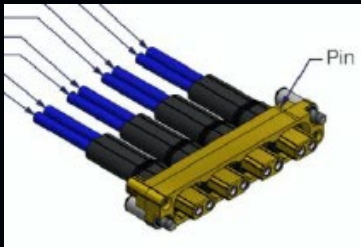
VCSEL driver array

Wireline Vs Optical

- FD 4m 400G link based on space grade wireline 3.125 Gb/s data lanes
- Cable assembly: SC25SP 17 grams/meter, 2.5 mm Ø & 1.55 dB/m @ 5 GHz (ESCC 3409/001 iss.4)



Electrical



ESCC3409/001
AxoMach


	Electrical	Optical	% decrease
Cables required	512	4	99.2
Cable mass (kg)	34.8	0.56	98.4
Cable volume (cm³)	10.000	113	98.8
Connector mass (kg)	3.84	0.114	97.0
TRx mass (kg)	-	0.05	-
Total mass (kg)	38.64	0.724	98.1

Optical



Space heritage
Q-MTitan

The OTRx is the critical element of space-grade on-board optical interconnects

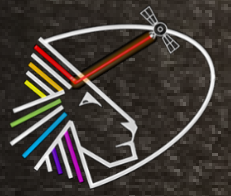


SIPhodiAS

Photonic-Enabled VHTS

www.space-siphodias.eu

[SIPHODIAS]: Space-grade Opto-electronic Interfaces for Photonic Digital & Analogue Very-high-throughput Satellite Payloads.



LEO SPACE PHOTONICS



Project lead – IC design

IC design & foundry

ALTER

Module AIT

ThalesAlenia
a Thales / Leonardo company
Space

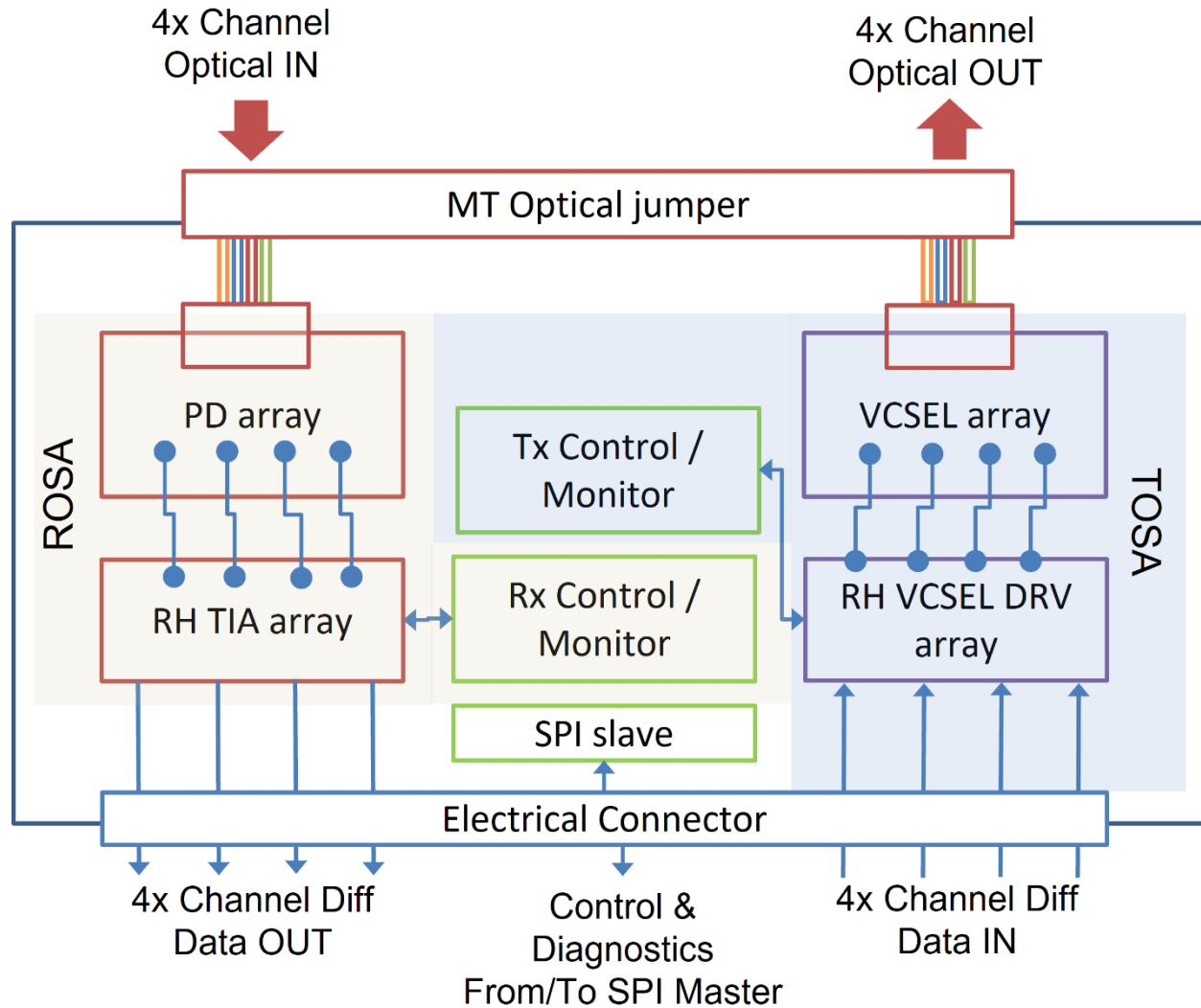
System specs & test



European
Commission

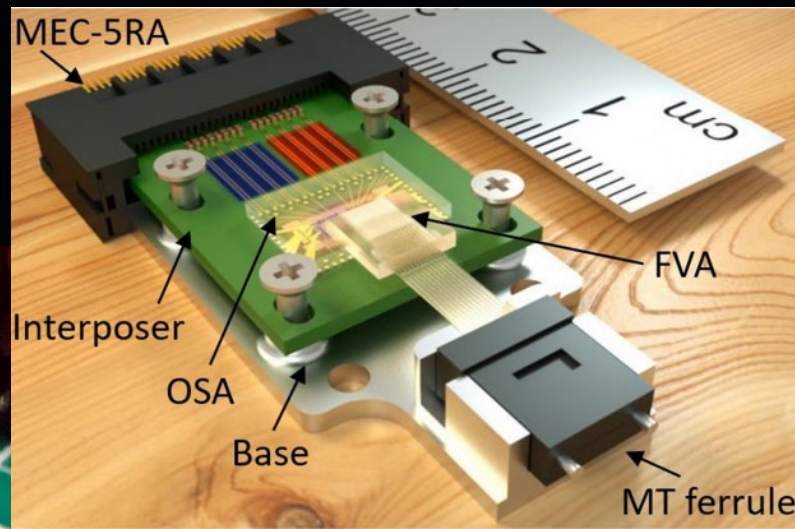
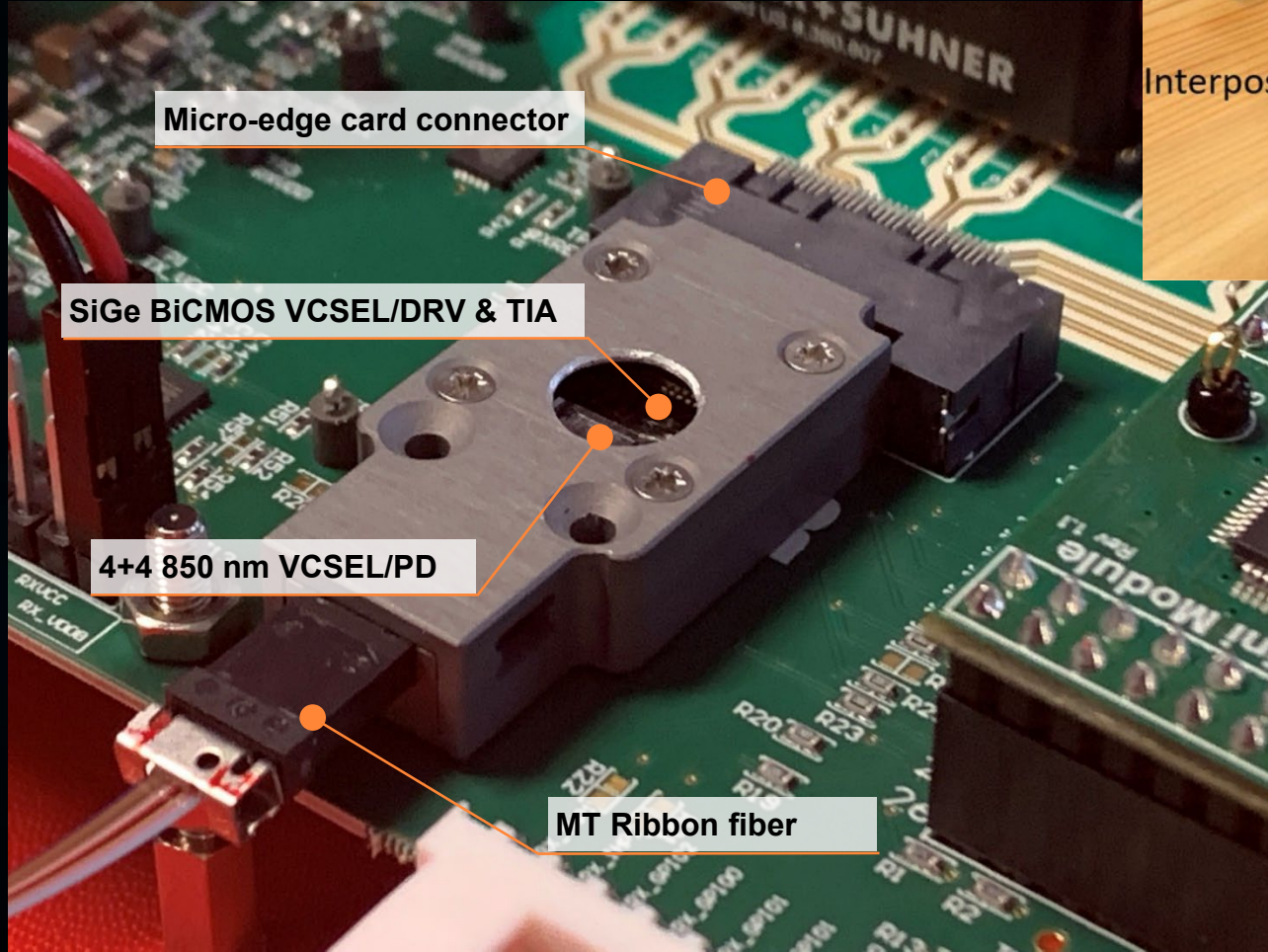
Horizon 2020
European Union funding
for Research & Innovation

OTRx Overview



OTRx features	
# of channels	4 Tx + 4 Rx
Opto-parts	1x4 850 nm MM VCSEL/PD
Electronic IC	Quad VCSEL DRV/TIA w/ RH SPI slaves
EIC technology	IHP SG13RH RH 130 nm SiGe BiCMOS
Electrical interface	Micro-edge card connector
Optical interface	MT ribbon 50/125 MMF

OTRx Module



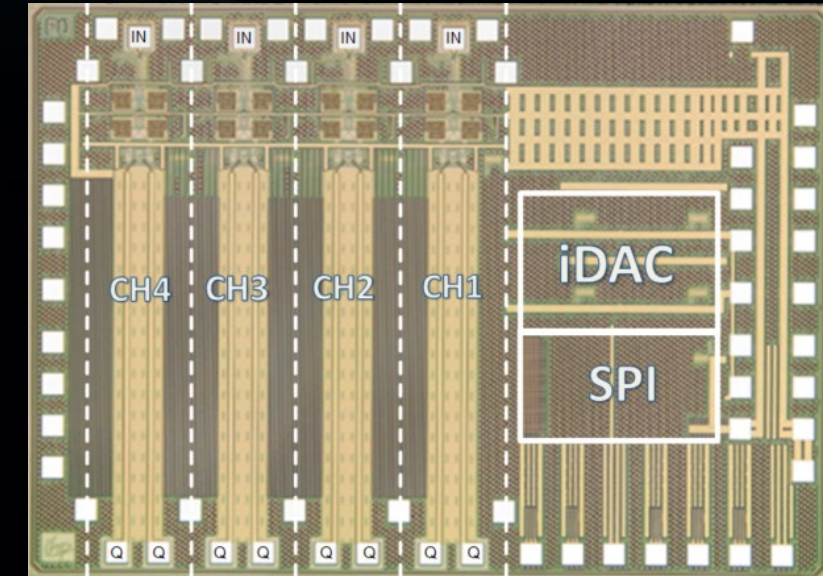
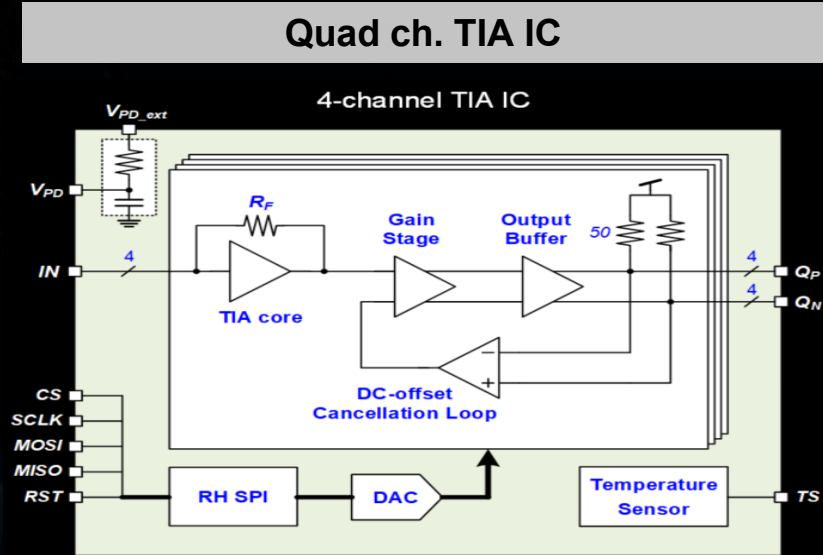
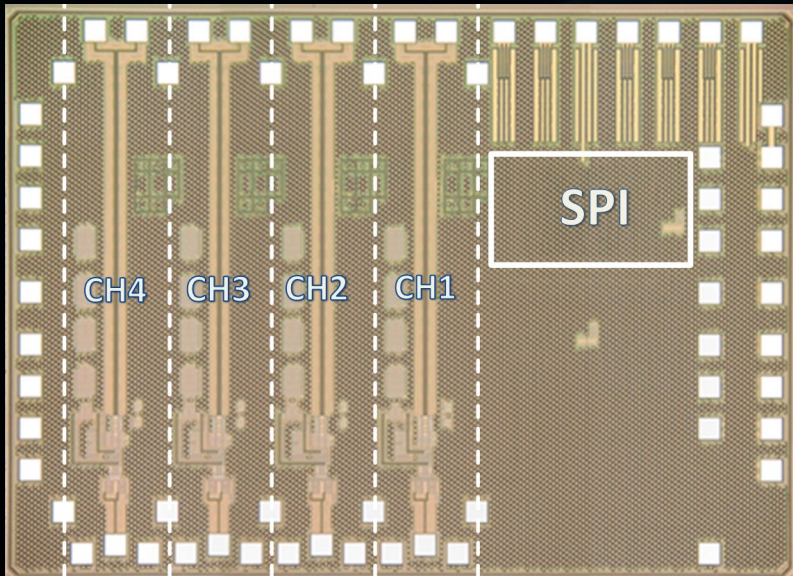
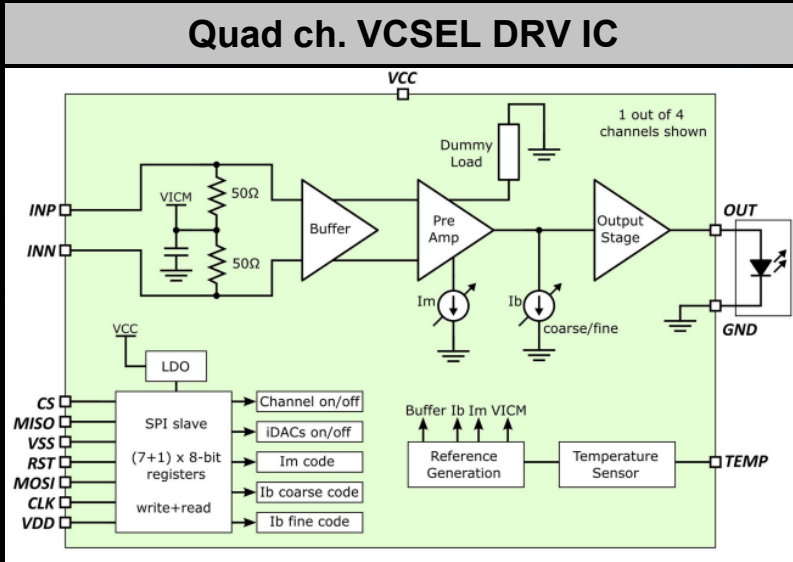
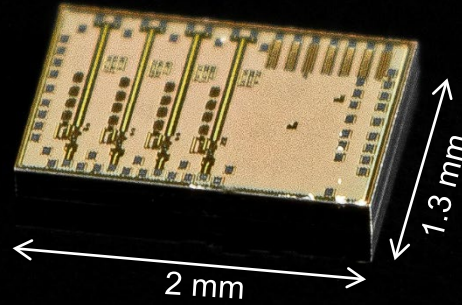
- All flip-chip assembly
- No BGA
- No interposer



OTRx mechanical & electrical specs	
Package size (LxWxD)	39.4 x 17 x 7.2 mm
Module footprint	670 mm ²
Module mass	6.4 grams (ex MEC & fiber)
Power supply	3.3 V
Power consumption	178 mW/channel
Target efficiency	< 7 mW/Gb/s

OTRx Chipset

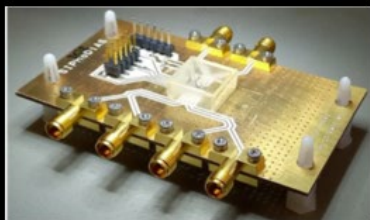
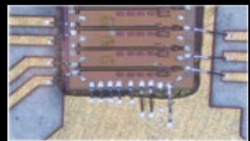
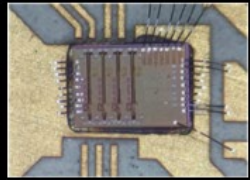
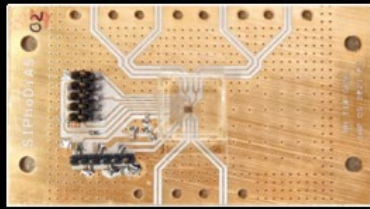
2.6 mm²



- IHP SG13RH process
- Single 3.3V power supply
 - RH bandgap circuit
 - RH SPI IP + DAC
 - Temperature sensor
- Programmable 4-channel O/P
 - VCSEL DRV: 70 mW/ch
 - TIA: 108 mW/ch

Verification Test Flow

Electrical Tests



PCB pre-assembly

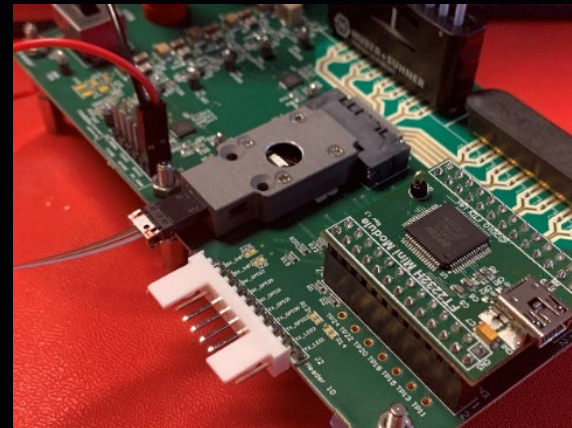
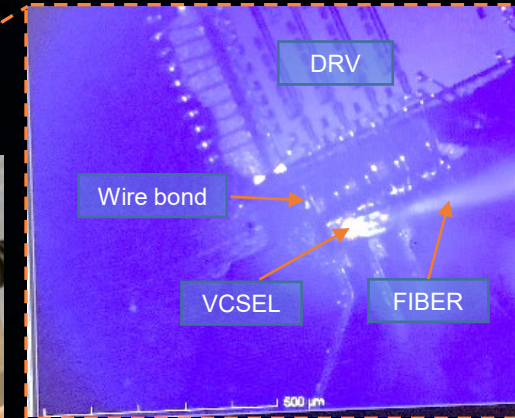
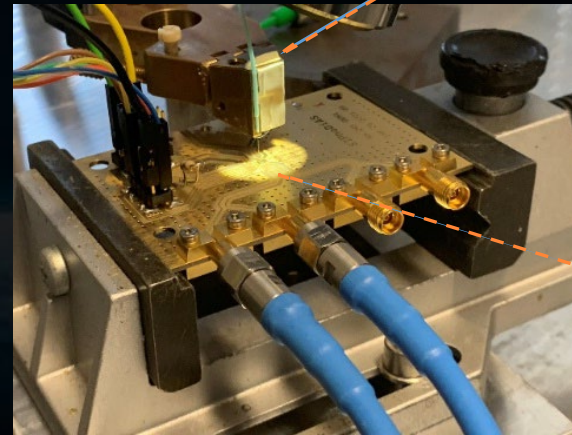
IC pre-wirebonding

Probe station
measurements

IC wire bonding

PCB assembly

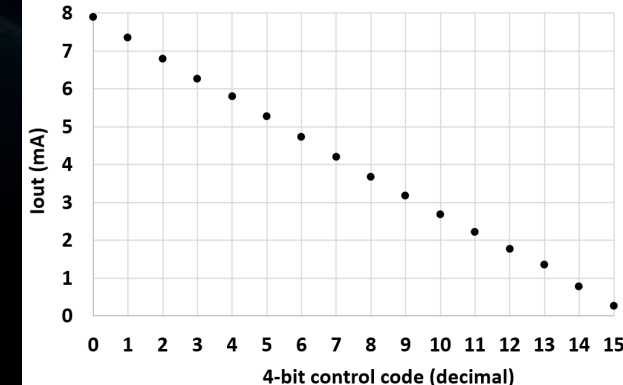
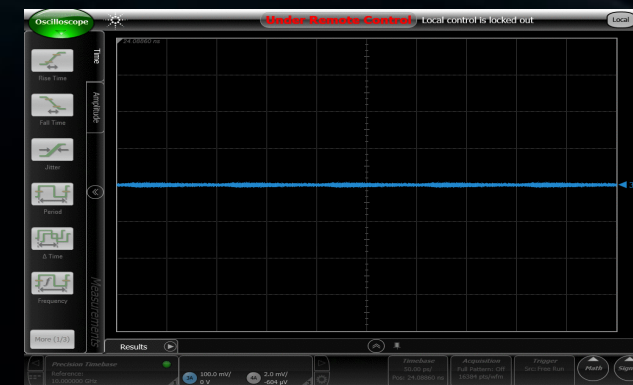
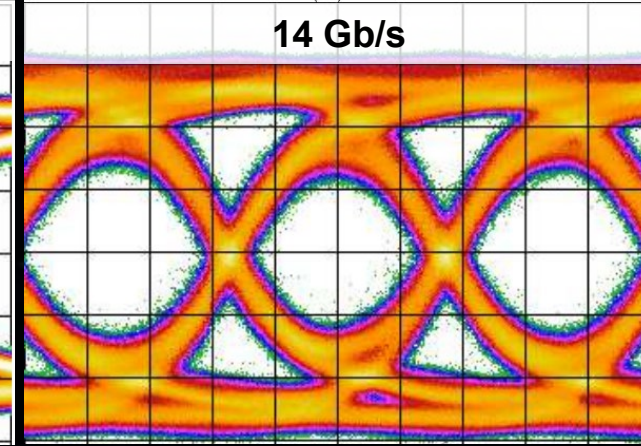
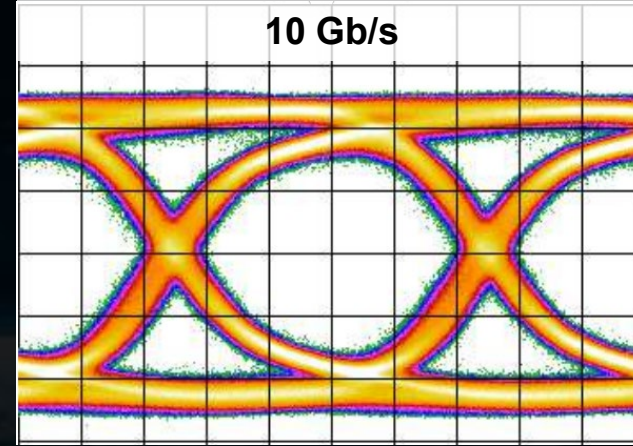
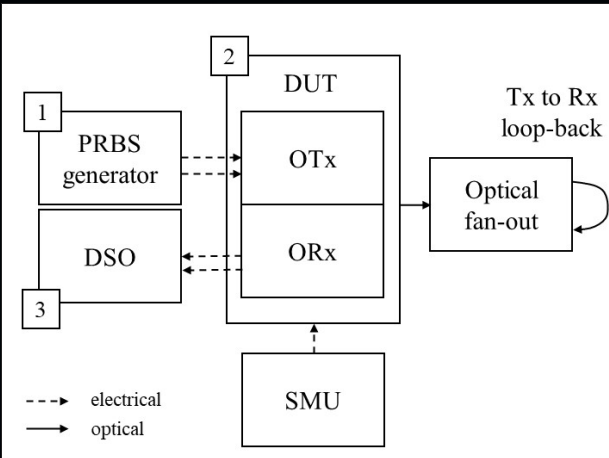
Opto-electronic Tests



EIC – VCSEL/TIA wire
bonding

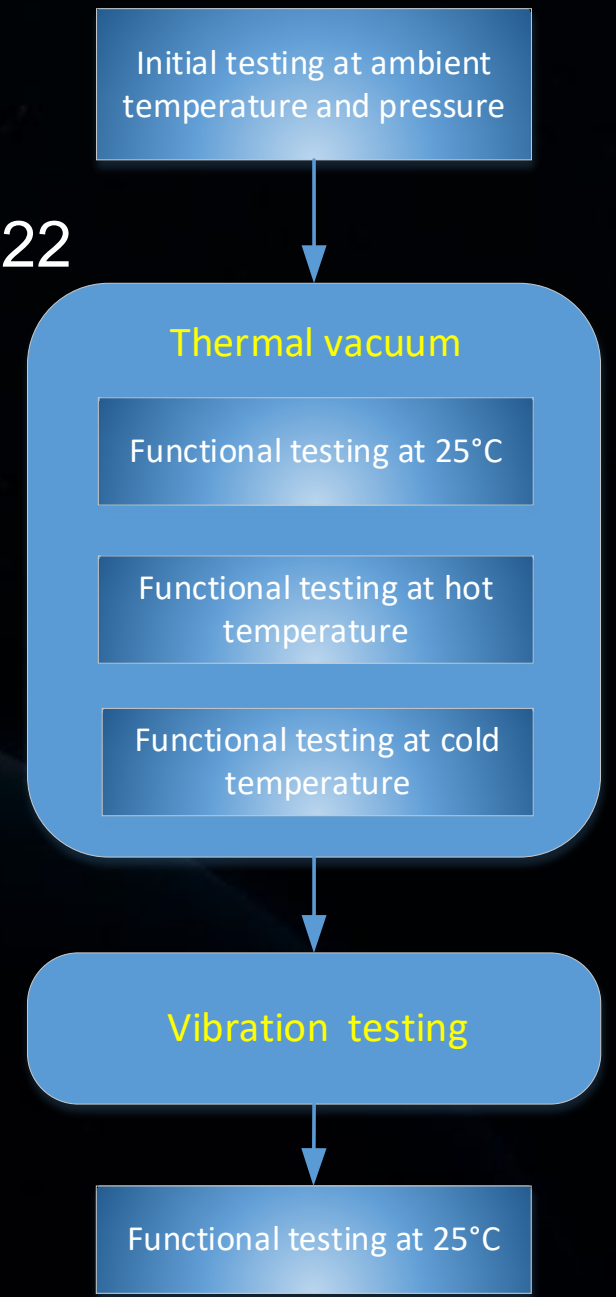
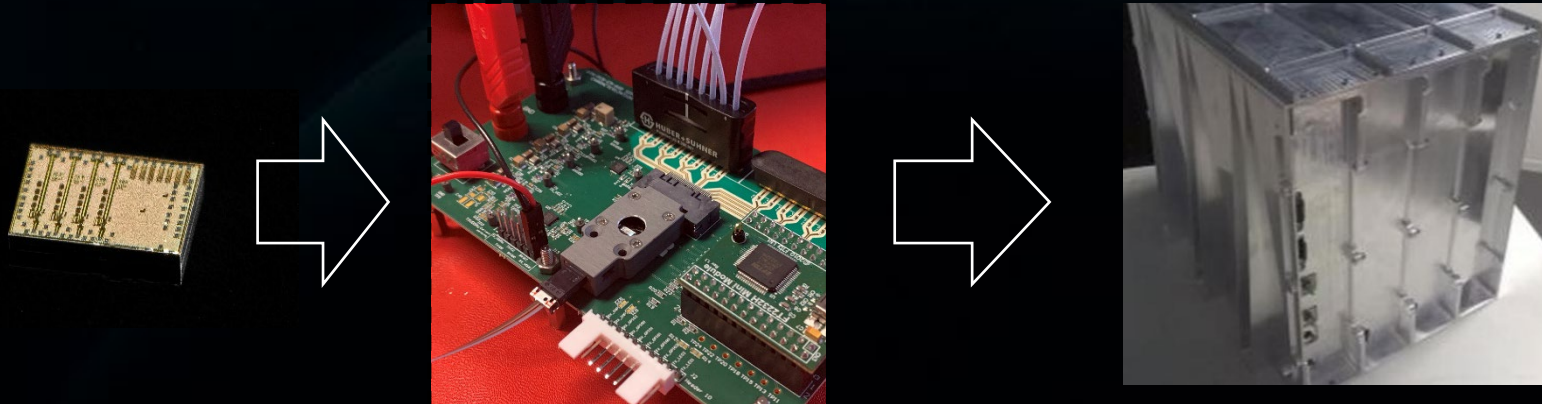
Full OTRx test

OTRx FFT Preliminary Results



NEXT STEPS

- VCSEL driver and TIA chipset v2 in fab – Available Dec. 2022
- SEE testing
- Module-level reliability testing
- System-level evaluation testing as per ECSS-E-ST-10-03C
 - TVAC
 - Random vibration



CONCLUSION

- New prototype OTRx for intra-satellite optical interconnects
 - RH-EIC co-designed with O/E for low power
 - All-flip-chip module assembly
 - Micro-edge connector for board assembly

Acknowledgment

European Union (EU) for funding through the “Horizon 2020” framework

- H2020-SPACE-SIPHODIAS – GA number 870522



Horizon 2020
European Union funding
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